UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,087	01/14/2004	Arup Bhattacharyya	MI22-2473	2443

21567 7590 02/03/2006

WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
3663	

DATE MAILED: 02/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,087	BHATTACHARYYA, ARUP	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *71-73,76 and 78-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *71-73,76 and 78-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 11/28/05 forms the basis for this office action. In said Amendment Applicant cancelled claims 74, 75, 77 and 80. Claims 1-70 and 82-88 had been cancelled previously. Applicant substantially amended all remaining claims 71-73, 76 and 78-81 at least through substantial amendment of claim 71. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement (IDS) filed 11/28/05. A signed copy of Form PTO-1449 is herewith enclosed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claim 71*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi (6,649,980 B2) in view of Shou et al (5,774,008).

Noguchi teaches an inverter (CMOS inverter; col. 3, l. 62) coupled with a signal source ("coupled with a signal source" is inherent to an inverter as otherwise there is no signal to invert), configured to invert the data signal and arranged to output the inverted

signal (the limitation "arranged to output the inverted signal" is inherently met because without output the inverter is not functional), the inverter including (cf. Figure 10):

a structure (comprising layers 101/102/103/104/109/106/107/108/110) (col. 12, l. 8-46) comprising silicon through for example 104, 107, and 110 (cf. col. 12, l. 12-20), and comprising germanium through 106 and 108 (col. 12, l. 16);

a first transistor supported by the structure, the first transistor comprising a first gate 106 (col. 12, l. 16) and a first active region 104 (col. 12, l. 8-15) (cf. Figure 10); the first active region including a first channel region (loc.cit.) and a pair of source and drain regions (col. 12, l. 8-27); at least a portion of the first active region being within the structure (all of it is, cf. Fig. 10), the first transistor being one of either a PFET or an NFET (col. 12, l. 58-64) and the first source/drain regions accordingly (inherently, that is: the channel's conductivity type is defined by the adjective p-type and the adjective n-type for PFET and NFET, respectively) being p-type doped regions or n-type doped regions, respectively;

a layer of semiconductor material 107 (col. 12, l. 8-46; please note especially col. 12, l. 41-46) over the first transistor and a second layer of semiconductor material over the first layer formed physically contacting the first layer of semiconductor material and the second layer of semiconductor material being compositionally different from the first layer of semiconductor material (col. 12, l. 41-46 disclosing inter alia *stepwise* variation of the *germanium content* from the upper side to the lower side of 106/107/108);

a second transistor (gate 108, active region 110) supported by the first and second layers of semiconductor material (namely: supported by the interconnection

between the SiGe gates 106 and 108), the second transistor comprising a second gate 108 (col. 12, l. 16) and a pair of second source/drain regions (within 110; cf. col. 12, l. 22), the second transistor being an NFET or PFET dependent upon whether the first transistor is a PFET or NFET, respectively, and the second source/drain regions accordingly (i.e., inherently) being n-type or p-type doped regions (see comment in this regard overleaf on the conductivity type of source/drain regions being of the same as the transistor) ; the first and second gates being electrically connected to one another (through 107 (cf. col. 12, l. 16 and Fig. 10) and being in electrical connection with the signal source (see Fig. 2; col. 6, l. 55 – col. 7, l. 16; this limitation also holds inherently for this CMOS inverter as otherwise no input signal can be provided and nothing can be inverted); and one of the first source/drain regions being electrically with one of the second source/drain regions (through contact 111) and being in contact with one of the second source/drain regions (Figure 2, col. 6, l. 55- col. 7, l. 16 and col. 12, l. 22-27; this limitation holds inherently because in a CMOS inverter the output signal emanates from the common source/drain region).

Noguchi does not necessarily teach the limitation that said CMOS inverter is comprised in a computer and said computer to comprise a signal source arranged to provide a data signal with said inverter configured to invert that data signal.

However, it would have been obvious to include said limitation in view of Shou et al, who teach the advantageous inclusion of CMOS inverters in a computer (title, abstract, their claim 1 and col. 1, l. 5-38; see also Fig. 15 and col. 7, l. 36 – col. 8, l. 8). *Motivation* to include the teaching by Shou et al in the invention by Noguchi immediately

derives from the profitable application of said invention to the field of computers: Figure 15 contains in it exactly the CMOS inverter as defined by its electrical connections and its function is exactly as described by Noguchi. Therefore, *combination* only involves module substitution.

2. ***Claims 72-73 and 79-81*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi and Shou et al as applied to claim 71 above, and further in view of Fitzgerald et al (US 2002/0125471 A1). As detailed above, claim 71 is unpatentable over Noguchi in view of Shou et al. Neither Noguchi nor Shou et al teach the further limitation defined by claim 72.

However, it would have been obvious to include said limitation in view of Fitzgerald et al, who teach a strained silicon upper surface layer of the channel region in a PFET in contact with a relaxed silicon germanium layer (see [0033]) so as to dramatically increase electron mobility, and inherently thereby operational speed, the latter providing *motivation* to include the teaching by Fitzgerald in the invention by Noguchi. *Combination* of said teaching with said invention implies the inclusion of at least two sub-layers within 110, a lower layer of relaxed crystalline SiGe (see [0055] in Fitzgerald et al; thus meeting claim 80) with the percentage of germanium taught to be 30% or 40% (thus meeting claim 81), for the latter value hole mobility being saturating; see [0059]) and an upper strained layer of Si (thus meeting the further limitation of claim 73), thus meeting all claim limitations of claim 72 as dependent upon claim 71.

On claim 79: lattice mismatch is spread over a distance by silicon germanium buffer layer 502, which buffer layer, being by its gradual accommodation of lattice

constant at least partly relaxed. Therefore, some of the mismatch must reside in 502/506 including the interface between 502 and 506. Any lattice mismatch implies at least two different lattice constant values and hence two different lattices and related crystals. Therefore, the relaxed crystalline lattice in 502/506 is polycrystalline.

3. ***Claims 76 and 78*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi, Shou et al and Fitzgerald et al as applied to claim 72 above, and further in view of Chu et al (6,251,751 B1).

As detailed above, claim 72 is unpatentable over Noguchi in view of Shou et al and Fitzgerald et al. Neither Noguchi nor Shou et al nor Fitzgerald et al necessarily teach the further limitation defined by claim 72. However, the range of germanium concentration in the strained silicon comprising layer in FETs is not restricted to zero, as witnessed by Chu et al, who teach that the germanium content of the strained crystalline layer 16 (col. 2, l. 35-45) may be finite, namely: they teach a strained silicon germanium (SiGe) layer (col. 2, l. 35-45) (thus meeting claim 76) over and abutting a single crystal SiGe semiconductor layer 14 (col. 2, l. 24-29) (thus meeting claim 78; N.B.: please note Meyerson is incorporated by reference in Chu et al; also see previous office action). The range of germanium content claimed is thus found in the prior art.

Response to Arguments

Applicant's arguments filed 11/28/05 have been fully considered but they are not persuasive. In particular, the entire claim language has been substantially amended. Upon through consideration and search the new claims were found unpatentable over Noguchi in view of Shou et al and art already cited in the previous office action.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
January 29, 2006

JACK KEITH
SUPERVISORY PATENT EXAMINER